

MADNESS project

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Fault Tolerant Network Interfaces for NoCs

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Outline

- ❑ **Motivations**
- ❑ **Fault model**
- ❑ **Fault tolerant NI architecture**
- ❑ **Preliminary results**
- ❑ **Future work**



Motivations

- ❑ As CMOS technology scales down into the deep-submicron domain, the aspects of fault tolerance in complex NoC-based architectures play a role of increasing relevance.
- ❑ New types of malfunctions and failures (temporary and permanent faults)
- ❑ New methodologies and architectural solutions specific for NoCs should be explored

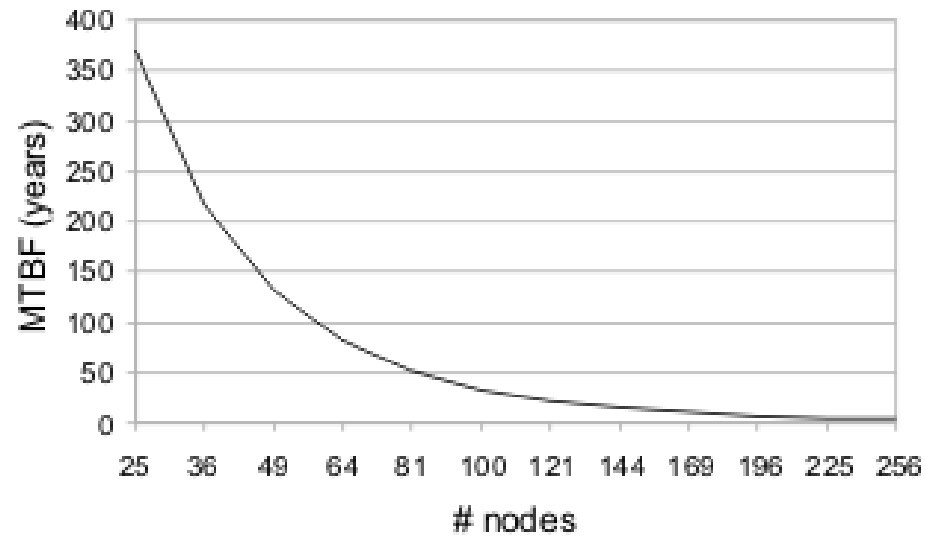


Motivations

- The NI represents a critical point in the design of fault tolerant NoCs:
 - Acts as interface between the core and the system
 - Error in NIs can directly affect the correct transmission of data and control information
 - Errors extremely hard to detect and recover without the appropriate support (for instance **deadlock** or **livelock**)
 - Faulty NIs can isolate working core (or cluster of cores) from the rest of the system
 - MTBF rapidly decreases as the dimension of the system increases (proportional to $1/N^2$)



Motivations



Motivations

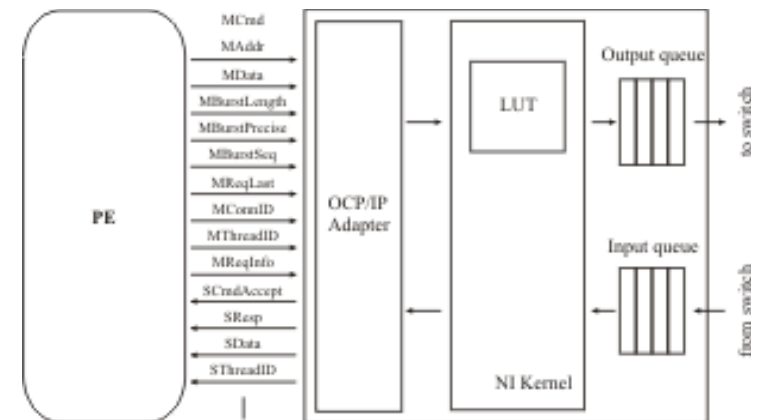
- In this work, we target:
 - Temporary faults
 - Permanent faults

- Contributions of this work:
 - To propose a functional fault model for NIs
 - To propose and evaluate a two-level architectural approach for NI's components employing a limited amount of redundancy



Fault model

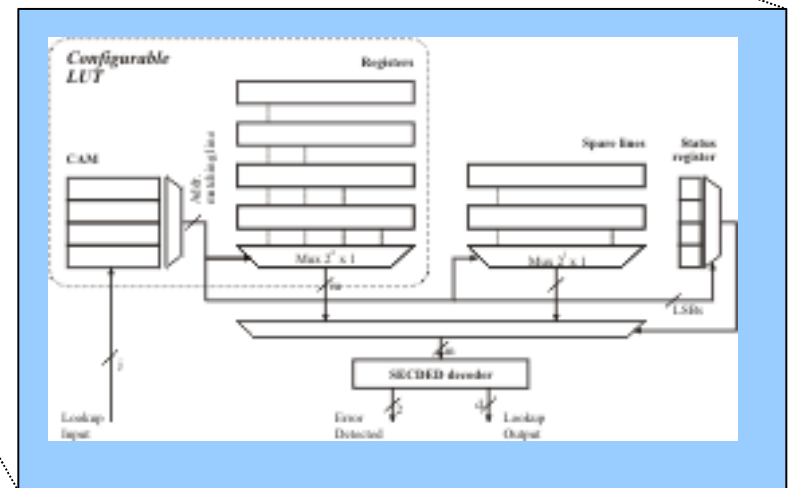
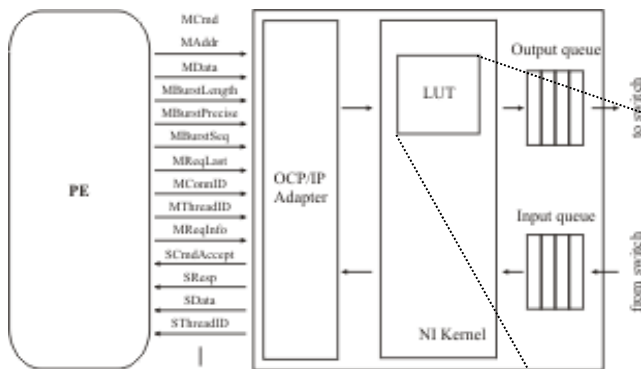
- Functional fault model:
 - Corrupt Data Fault
 - Corrupt Protocol Conversion Fault
 - Routing Path Fault
 - Multiple Copies-in-Time Fault



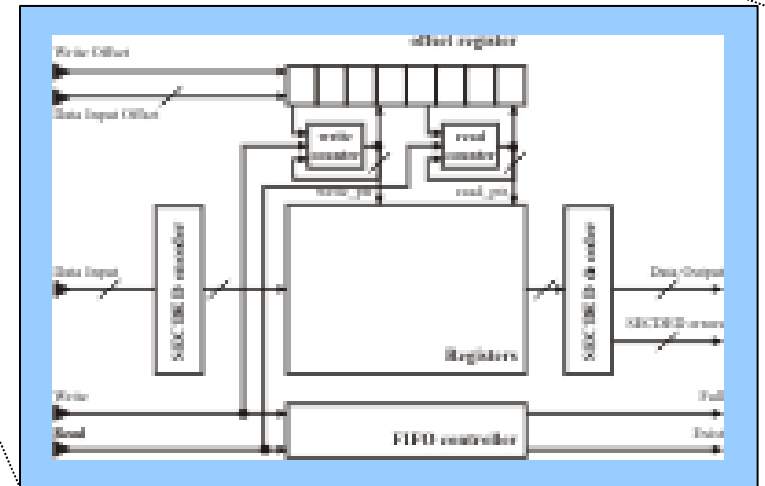
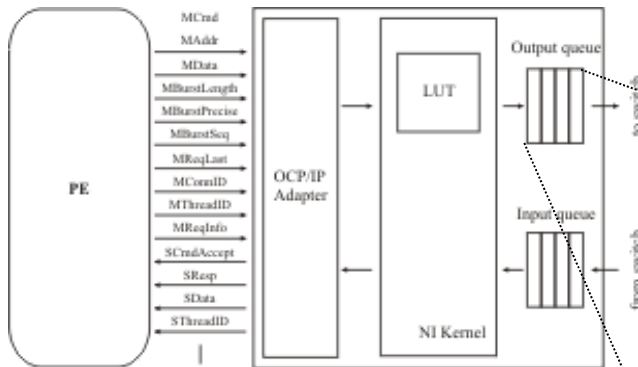
- Focus on LUT, FIFOs, and FSMs



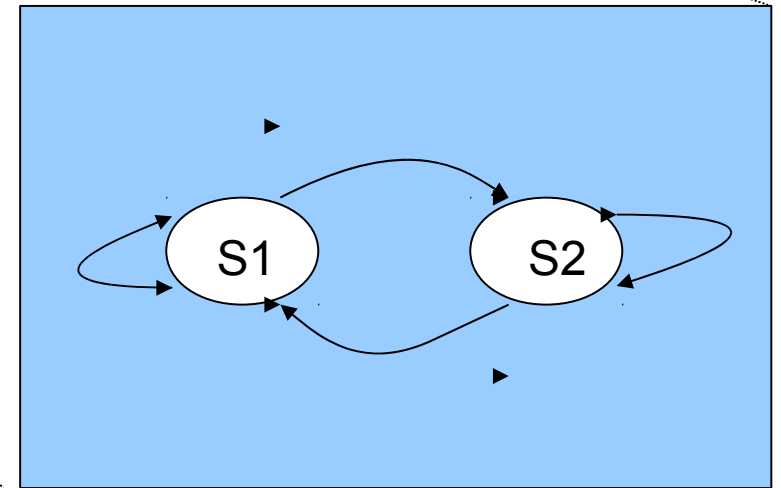
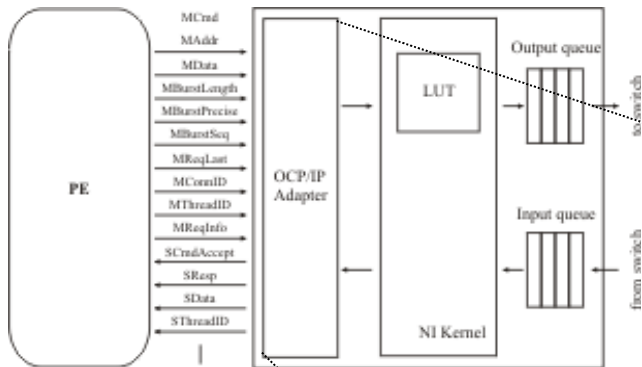
Fault tolerant NI architecture: LUT



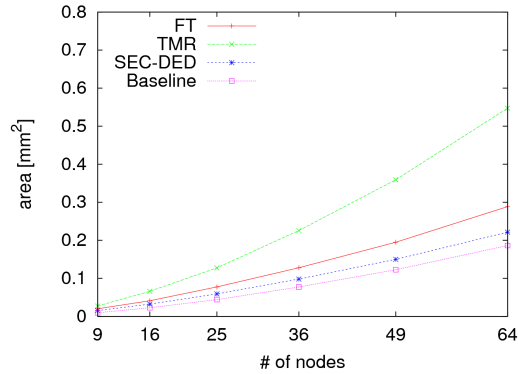
Fault tolerant NI architecture: FIFO



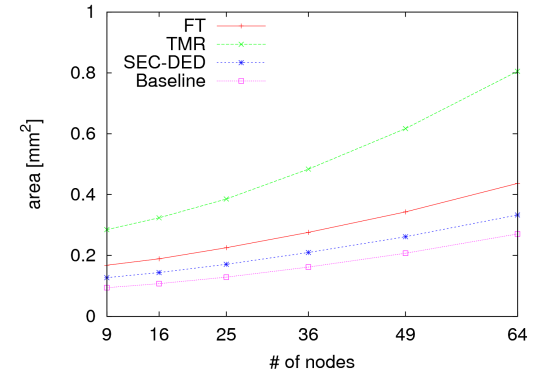
Fault tolerant NI architecture: FSMs



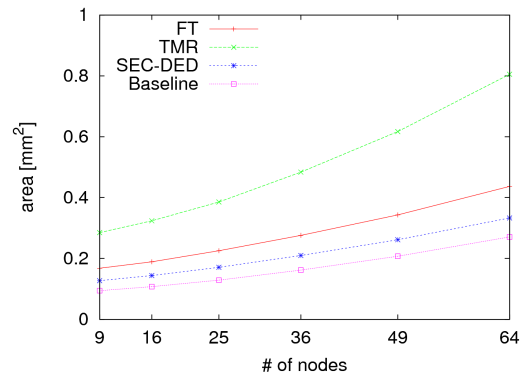
Preliminary results: area



LUT



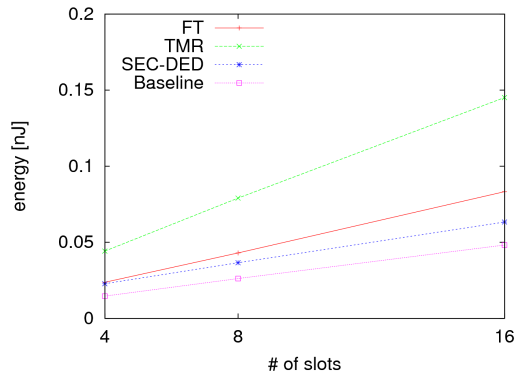
FIFO



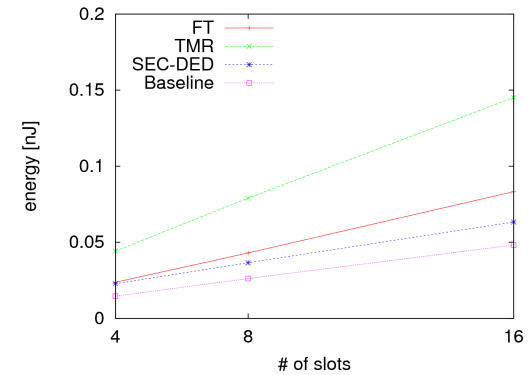
NI



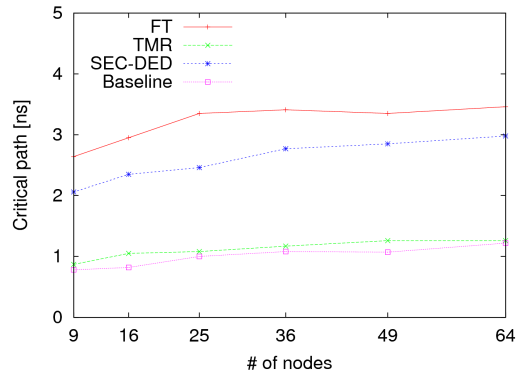
Preliminary results: energy & critical path



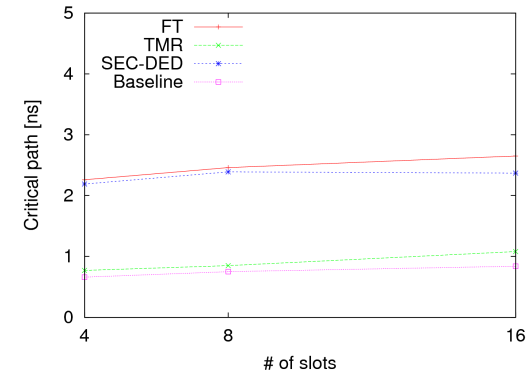
LUT



FIFO



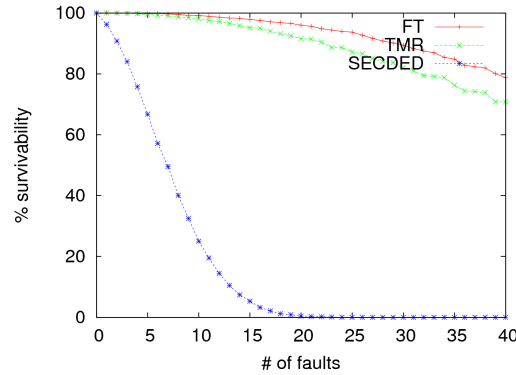
LUT



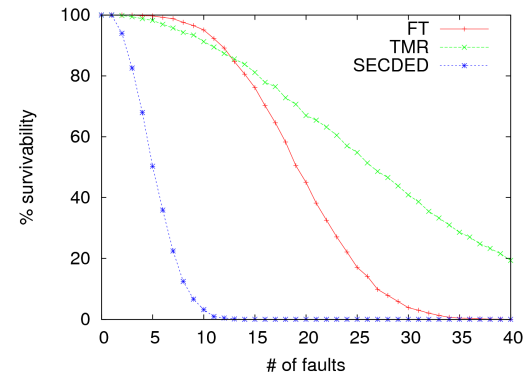
FIFO



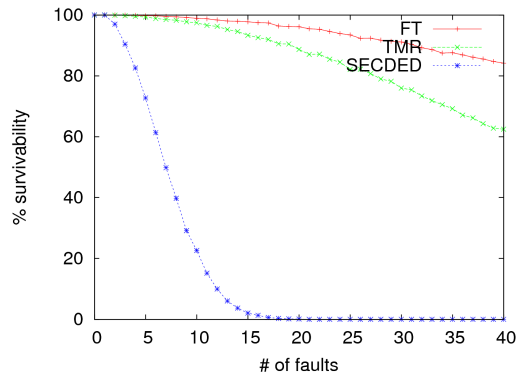
Preliminary results: survivability



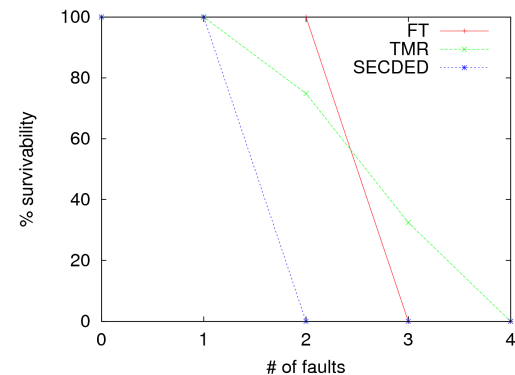
NI



LUT



FIFO



FSM



Conclusions and future work

- ❑ We proposed a functional fault model for the Network Interface
- ❑ We evaluated alternative architectural fault tolerant solutions for the NI and its components, based on the use of SECDED codes in combination with limited architectural redundancy
- ❑ We analyzed overhead of the proposed solutions with respect to alternative implementations: we obtained a saving of 83% in the area overhead as well as a significant energy reduction with respect to an alternative TMR implementation, while maintaining a similar level of robustness to faults
- ❑ Main drawback: increased critical path due to Hamming decoder
- ❑ Future work will focus on the optimization of the implementation of the SECDED decoder, on the study of reconfiguration policies for employing architectural redundancy at run-time, on extending the use of evaluated techniques to routers





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Thanks for your attention!

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